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Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (original) A method for sampling a digital signal yielding improved jitter performance within prescribed bandwidth constraints, comprising the steps of:

periodically sampling the digital signal n times during every interval t, with n chosen such that $\log_2(n+1)$ is an integer (x) greater than zero;

generating a $x+1$-bit sample value after each interval t, the sample value having a first bit indicating the value of the digital signal being sampled, and x remaining bits which collectively indicate a sample interval during which the digital signal changed states if such a change did occur, and

inverting the first bit of each sample value upon decoding to coincide with the change in the digital signal.

2. (original) The method according to claim 1 wherein $n=15$ and x equals 4.

3. (currently amended) An ~~A~~apparatus for sampling a digital signal yielding improved jitter performance within prescribed bandwidth constraints, comprising ~~of~~:

a sample clock for generating n periodic clock pulses during every interval t, with n chosen such that $\log_2(n+1)$ is an integer (x) greater than zero;

a receiver for generating a $x+1$-bit sample value after each interval t, the sample value having a first bit indicating the value of the digital signal being sampled, and x remaining bits which collectively indicate a sample interval during which the digital signal changed states if such a change did occur, and the receiver inverting the first bit of each sample value upon decoding to coincide with the change in the digital signal.

4. (original) The apparatus according to claim 1 wherein $n=15$ and x equals 4.

5 (previously presented) A method for sampling a digital signal yielding improved jitter performance within prescribed bandwidth constraints, comprising the steps of:

periodically sampling the digital signal n times during every interval t, with n chosen such that $\log_2(n) =< x$ where x is an integer;

generating a x+1-bit sample value after each interval t, the sample value having a first bit indicating the value of the digital signal being sampled, and x remaining bits which collectively indicate a sample interval during which the digital signal changed states if such a change did occur, and

inverting the first bit of each sample value upon decoding to coincide with the change in the digital signal.

6. (previously presented) The method according to claim 5 wherein n=15 and x equals 4.

7. (currently amended) An ~~A~~apparatus for sampling a digital signal yielding improved jitter performance within prescribed bandwidth constraints, comprising ~~of~~:

a sample clock for generating n periodic clock pulses during every interval t, with n chosen such that $\log_2(n) =< x$ where x is an integer

a receiver for generating a x+1-bit sample value after each interval t, the sample value having a first bit indicating the value of the digital signal being sampled, and x remaining bits which collectively indicate a sample interval during which the digital signal changed states if such a change did occur, and the receiver inverting the first bit of each sample value upon decoding to coincide with the change in the digital signal.

8. (new) The apparatus according to claim 7 wherein n=15 and x equals 4.